AMENDMENTS TO THE CLAIMS

1. (currently amended) An anti-wafer structure for testing a plurality of dice on a wafer under test, the structure comprising:

a silicon on insulator (SOI) layer;

a plurality of probe dice formed on the SOI layer, each probe die in the plurality of probe dice having a pad layout corresponding to a pad layout of a die on the wafer under test;

a plurality of holes, each of the holes extending through the SOI layer and a probe die in the plurality of probe dice, the holes corresponding to pads on the plurality of probe dice;

wherein the holes are filed with interconnect lines coupled to form electrical connections on either side of the anti-wafer structure.

2. (canceled)

3. (canceled)

4. (previously presented) The anti-wafer structure of claim 1 wherein the interconnect lines are coupled to pads of the wafer under test.

5. (original) The anti-wafer structure of claim 1 wherein a number of the probe dice equals a number of dice on the wafer under test.

6. (original) The anti-wafer structure of claim 1 wherein the SOI layer comprises an oxide layer.

7-11. (canceled)

12. (currently amended) A method of fabricating an anti-wafer, comprising:

providing a substrate, a silicon on insulator (SOI) ~~an SOI~~ layer over the substrate, and a silicon layer over the SOI layer;

forming a seal layer over the silicon layer;

removing the substrate using a polishing process;

forming an opening through the SOI layer and the silicon layer;

removing the seal layer;

forming an interconnect line extending through the SOI layer and the silicon layer;

performing an HF dip process to clean a surface of the SOI layer after the polishing process.

13-15 (canceled)

16. (previously presented) The method of claim 12 further comprising:

depositing an oxide on the SOI layer after the HF dip process.

17. (original) The method of claim 12 wherein the seal layer comprises:
an oxide layer over the silicon layer; and
a nitride layer over the oxide layer.

18. (original) The method of claim 12 wherein the silicon layer includes pad openings and the seal layer protects the pad openings during subsequent processing steps.

19. (original) The method of claim 12 wherein the SOI layer comprises silicon dioxide.

20. (original) The method of claim 12 wherein the substrate comprises a silicon substrate.

21. (previously presented) An anti-wafer structure for testing a plurality of dice on a wafer under test, the structure comprising:
a silicon on insulator (SOI) layer;
a plurality of probe dice formed on the SOI layer, each probe die in the plurality of probe dice having a pad layout corresponding to a pad layout of a die on the wafer under test; and
an adapter layer configured to adapt a pad layout of a probe die to another pad layout.

22. (previously presented) The anti-wafer structure of claim 21 further comprising:
a plurality of holes extending through the SOI layer and the plurality of probe dice, the holes corresponding to pads on the plurality of probe dice.

23. (previously presented) The anti-wafer structure of claim 22 wherein the holes are filed with interconnect lines coupled to form electrical connections on either side of the anti-wafer structure.

24. (previously presented) The anti-wafer structure of claim 23 wherein the interconnect lines are coupled to pads of the wafer under test.

25. (previously presented) The anti-wafer structure of claim 21 wherein a number of the probe dice equals a number of dice on the wafer under test.

26. (previously presented) The anti-wafer structure of claim 21 wherein the SOI layer comprises an oxide layer.